REMARKS

Claims 1-4 are pending in the present application. Claims 1- 4 have been amended.

Priority Under 35 U.S.C. 119

A Claim of Priority Letter and a certified copy of priority application No. 2002-354726 have been filed along with the present application on October 21, 2003. The Claim of Priority Letter and certified copy of the priority application have been entered into the image file wrapper of the present application on the U.S. Patent Office website. **The Examiner is respectfully requested to acknowledge receipt of the certified copy of the priority document, and to confirm on the record that the Claim for Priority Under 35 U.S.C. 119 is complete**.

Claim Rejections-35 U.S.C. 112

Claim 4 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 4 has been amended to feature in combination "a process of writing in a first address in said memory a jump instruction to jump to a second address in said memory". Applicant respectfully submits that claim 4 is in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

Claim Rejections-35 U.S.C. 103

Claims 1-3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (characterized as Admission by the Examiner) in view of the Katsuta reference (U.S. Patent No. 5,671,394). This rejection is respectfully traversed for the following reasons.

The microcomputer of claim 1 includes in combination a first memory; a second memory; a test mode detection circuit; a central processing unit (CPU) "which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated"; a memory management unit; and a test circuit "which gives a preset specific instruction to said CPU when, in said test mode, a security test signal has been output from said CPU and a specific memory area has been accessed". Applicant respectfully submits that the microcomputer of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has alleged that Applicant's admitted prior art discloses a test circuit "which gives a preset specific instruction to said CPU when, in said test mode, a specific memory has been accessed. (figure 2, item 8; page 4, line 4 – page 5, line 13)".

Applicant however respectfully submits that test circuit 8 of Applicant's admitted prior art Fig. 2 is not disclosed as giving a preset specific instruction to a CPU, in a test mode, **when a specific memory area has been accessed**, as would be necessary to

meet the features of claim 1. That is, page 4, line 4 through to page 5, line 13 of the present application does not specifically describe that test circuit 8 is operable responsive to access of a specific memory area. Test circuit 8 in Applicant's admitted prior art Fig. 2 is responsive to test mode signal TM, test instructions connected to test signal input terminals 8a and read data RDT read from ROMs 2 and 3, and RAM 4. Test circuit 8 of Applicant's admitted prior art Fig. 2 does not include an address decoder function. Accordingly, contrary to the Examiner's assertion, test circuit 8 of Applicant's admitted prior art Fig. 2 does not give a preset specific instruction to the CPU when a specific memory area has been accessed. Applicant therefore respectfully submits that Applicant's admitted prior art does not meet the features of claim 1 as asserted by the Examiner, and that this rejection of claims 1 and 2 is improper for at least these reasons.

With further regard to claim 1, the Examiner has acknowledged that Applicant's admitted prior art does not explicitly disclose a security test signal output from a CPU. In an effort to overcome this acknowledged deficiency, the Examiner has asserted that column 3, line 26 through to column 4, line 55 of the Katsuta reference discloses a security test signal output from a CPU, and that it would have been obvious to modify Applicant's admitted prior art in view of the Katsuta reference. Applicant respectfully disagrees for the following reasons.

Applicant respectfully submits that column 3, line 26 through to column 4, line 55 of the Katsuta reference does not disclose a CPU that outputs a security test signal,

and more particularly does not disclose a CPU that outputs a security test signal to a test circuit, as would be necessary to make obvious the features of claim 1. In general, the single-chip microcomputer shown in Fig. 1 of the Katsuta reference compares an input data from input port 5 with key data read from ROM 4 as a security check. As described in column 3, lines 56-65 of the Katsuta reference, CPU 1 initializes a start address in ROM 4 to "UADR", or in the alternative initializes a start address in ROM 4 to "TADR". CPU 1 thus outputs addresses to access user or test areas of ROM 4, which is shown in detail in Figs. 2-3. CPU 1 is not specifically described as outputting a security test signal through a test circuit. That is, a security test signal and a test circuit are not specifically shown in Fig.1 or described in column 3, line 26 through to column 4, line 55 of the Katsuta reference as generally relied upon by the Examiner. The Katsuta reference as secondarily relied upon therefore does not overcome the acknowledged deficiencies of Applicant's admitted prior. Accordingly, Applicant respectfully submits that the microcomputer of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1 and 2 is improper for at least these reasons.

The microcomputer of claim 3 includes in combination among other features an exception processing circuit "included in said CPU, for executing a predetermined exception process when said functional test program is executing a security test and said memory management unit has instructed execution of said specific operation".

Applicant respectfully notes that the Examiner has not established how

Applicant's admitted prior art Fig. 2 and/or the Katsuta reference as secondarily relied may be interpreted as disclosing or suggesting an exception processing circuit as featured in claim 3. The Examiner has failed to address the exception processing circuit in the rejection, and thus has apparently disregarded these features of claim 3. Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious an exception processing circuit as featured in claim 3. Applicant therefore respectfully submits that the microcomputer of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 3 is improper for at least these reasons.

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of the Mendell reference (U.S. Patent No. 4,519,032). This rejection is respectfully traversed for the following reasons.

The Examiner has alleged that page 2, lines 23-27 of the present application, as descriptive of Applicant's admitted prior art, discloses a process of determining "if there is a failure depending on whether or not said memory management unit has output from said interrupt signal as a result of executing said jump instruction written at said first address".

Applicant respectfully submits that page 2, lines 23-27 of the present application, as descriptive of Applicant's admitted prior art, does not describe determining a failure, as asserted by the Examiner. Specifically, page 2, lines 23-27 of the present

application describes executing a specific instruction in an application program; and inhibiting an access and jump or the like to a specific area, so as to protect against downloading of an illegitimate program and reading and writing of data such as a password or a private key. There is no discussion or suggestion of failure determination on page 2, lines 23-27 of the application. Applicant's admitted prior art does not disclose the features as suggested by the Examiner. Applicant therefore respectfully submits that this rejection of claim 4 is improper for at least these reasons.

With further regard to claim 4, the Examiner has acknowledged that Applicant's admitted prior art does not explicitly disclose a process of jumping to a first address. In an effort to overcome this acknowledged deficiency, the Examiner has alleged that the Mendell reference discloses a process of jumping to a first address in column 4, lines 42-58.

Processor 200 as shown in Fig. 2 of the Mendell reference is specifically described beginning in column 4, line 42 as containing an interrupt input, and an interrupt controller that operates under control of an interrupt program. As described in column 4, lines 39-41 of the Mendell reference, the interrupts are generated on illegal reads/writes or on attempted accesses to memory that is out of the allocated address range. Column 4, lines 42-58 of the Mendell reference as specifically relied upon does not describe testing. This portion of the Mendell reference as relied upon generally describes a jump from an instruction set currently being executed to a new instruction set. Since this particular portion of the Mendell reference does not appear to be

specifically concerned with testing, one of ordinary skill would have no motivation to modify Applicant's admitted prior art in the manner suggested by the Examiner. Applicant therefore respectfully submits that the test method of claim 4 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 4 is improper for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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